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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte BURKHARD BECKER

Appeal 2009-008459
Application 10/730,619
Technology Center 2100

Before JOSEPH L. DIXON, HOWARD B. BLANKENSHIP, and JEAN R. HOMERE, *Administrative Patent Judges.*

DIXON, *Administrative Patent Judge.*

DECISION ON APPEAL[1]

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

The Appellant appeals under 35 U.S.C. § 134(a) from the Final Rejection of claims 1-3, 5-8, 11-15, and 18-23. Claim 4 has been canceled. Claims 9, 10, 16, 17 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewriting claims 9, 10, 16, and 17 in independent form including all of the limitations of the base claims 1 and 11, and any intervening claims. We have jurisdiction under 35 U.S.C. § 6(b).

We REVERSE.

I. STATEMENT OF THE CASE

The Invention

The invention at issue on appeal relates to a method and a device for transmitting data between a processor and an Arithmetic-Logic Unit (ALU) (Spec. 1).

The Illustrative Claim

Claim 1, an illustrative claim, reads as follows:

> 1. A method for transmitting data of a plurality of data types between a digital processor and a hardware arithmetic-logic unit, the method which comprises:
>
> associating the hardware arithmetic-logic unit with at least one table memory, the hardware arithmetic-logic unit obtaining data required during a computing operation from the table memory and/or the hardware arithmetic-logic unit storing data computed during a computing operation in the table memory;

reading and/or writing from the digital processor to the table memory by:

preselecting a base address in the table memory dependent on a data type of data to be transmitted;

computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware by taking the preselected base address as a starting point resulting in a computed plurality of addresses; and

accessing the table memory with the digital processor using the computed plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory; and

providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule.

The References

The Examiner relies on the following references as evidence:

Stafford	US 3,833,888	Sep. 3, 1974
Hess	US 4,405,980	Sep. 20, 1983
Tipon	US 5,150,471	Sep. 22, 1992
Serizawa	US 5,311,523	May 10, 1994

The Rejections

The following rejections are before us for review:

Claims 1-3, 5, 6, 11-15, 18, and 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hess and Tipon.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hess, Stafford, and Tipon.

Claims 8 and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Hess, Serizawa, and Tipon.

II. ISSUE

Has the Examiner erred in finding that the combination of Hess and Tipon teaches or fairly suggests "providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule" as recited in independent claim 1?

III. PRINCIPLES OF LAW

Obviousness

"Obviousness is a question of law based on underlying findings of fact." *In re Kubin*, 561 F.3d 1351, 1355 (Fed. Cir. 2009). The underlying factual inquiries are: (1) the scope and content of the prior art; (2) the differences between the prior art and the claims at issue; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations of nonobviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citation omitted).

IV. FINDINGS OF FACT

The following findings of fact (FFs) are supported by a preponderance of the evidence.

Hess

1. Hess discloses an address processor AR for processing the address and an ALU for process data:

> At the beginning of a program step, *the address processor AR* reads from the address memory AS*p* addresses which are processed to become addresses under which *the data to be processed in the present program step are stored in the main memory AKU.* Thereupon, *this data is successively read into the arithmetic logic unit ALU, processed,* that is, linked with each other, and at the end of the program step the result is fed, pulse-frequently driven, via the data bus to the data output unit I/O and/or the main memory AKU. *The data and its addresses are thus separately processed* and coordinated in accordance with the pulse control.

(col. 6, ll. 38-50, fig.2) (emphasis added).

V. ANALYSIS

The Appellant has the opportunity on appeal to the Board of Patent Appeals and Interferences (BPAI) to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) (citing *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

The Examiner sets forth a detailed explanation of a reasoned conclusion of unpatentability in the Examiner's Answer. Therefore, we look to the Appellant's Brief to show error in the proffered reasoned conclusion.

The Common Feature in Claims

Independent claim 1, recites, *inter alia*, "providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule." Independent claim 11, with different wording, contains these similar limitations.

35 U.S.C. § 103(a) rejections

With respect to independent claim 1, the Appellant contends that Hess fails to teach that "the ALU uses any type of arithmetic computation rule to compute addresses. Appellant points out that the ALU in Hess simply processes data that is received from the main memory AKU. The AKU taught by Hess does not even compute addresses." (App. Br. 7).

The Examiner states that "Hess clearly teaches providing an arithmetic computation rule as an incrementation rule or a decrementation rule" in order to compute addresses. (Ans. 12.) The ALU (fig.1) is a necessity for a computer to perform arithmetic and logic operations. *Id.*

We disagree with the Examiner's interpretation of the Hess reference. We find that the paragraphs and figures of the Hess reference upon which the Examiner relied only discuss an address processor to process the addresses and the ALU to process the data at the processed addresses. These two operations are separate operations (FF 1). Thus, even though, in general,

an ALU is a necessity for a computer to perform arithmetic and logical operations, the ALU disclosed in the Hess reference is used for processing the data, not addresses. We, therefore, find the Examiner's position is untenable.

Because we agree with at least one of the Appellant's contentions, we find that the Examiner has not made a requisite showing of obviousness as required to teach or fairly suggest the invention as recited in claim 1 by the combined teachings of Hess and Tipon that does not cure the noted deficienves of Hess. The rejection of the dependent claims 2, 3, 5, 6-8, and 23 contains the same deficiency. The Appellant, thus, has demonstrated error in the Examiner's reasoned conclusion for obviousness of the subject matter of claims 1-3, 5, 6-8, and 23

The independent claim 11 contains the similar limitations to those found in independent claim 1. The Appellant presents similar arguments as set forth with respect to independent claim 1 in response to the rejection of independent claim 11 (App. Br. 6-7).

As we found above in our discussion with respect to independent claim 1, we similarly find that the Appellant has demonstrated error in the Examiner's conclusion for obviousness of the subject matter of independent claim 1. The rejection of dependent claims 12-15 and 18-22 also contains the same deficiency. Hence, the Appellant's argument persuades us that the Examiner erred in rejecting claims 1-3, 5-8, 11-15, and 18-23.

We, therefore, cannot sustain the obviousness rejections of claims 1-3, 5-8, 11-15, and 18-23 under 35 U.S.C. § 103(a).

VI. CONCLUSION

We conclude that the Examiner erred by failing in identifying that the combination of Hess and Tipon teaches or fairly suggests "providing the arithmetic computation rule for computing the plurality of addresses in the table memory as an incrementation rule or a decrementation rule" as recited in independent claim 1.

VII. ORDER

We reverse the obviousness rejections of claims 1-3, 5-8, 11-15, and 18-23 under 35 U.S.C. § 103(a).

REVERSED

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